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A Technique for Improving Input Current Zero-crossing Distortion of Boost PFC Converters for Airborne System

Bin Zhou[1], Hongtao Shan[2]

[1] *(College of Mechanical Engineering, Shanghai University of Engineering Science, Shanghai, China)*
[2] *(College of Electronic and Electrical Engineering, Shanghai University of Engineering Science, Shanghai, China)*

Abstract : In airborne AC power system, input current may distort at the vicinity of input voltage zero crossing in Power Factor Correction (PFC) converter. This paper is analyzed the essential causes of the zero-crossing distortion and points out that the major causes are the value of inductor and the phase displacement between input current and input voltage. By adopting parallel interleaving technique, it can decrease the inductor and increase the equivalent switching frequency, improve input current zero-crossing distortion effectively. The effectiveness of this method is verified by simulation and experiments. The experiment results are demonstrated that it can make input current harmonics meet relevant standards so it can be applied in airborne system.

Key words- Airborne System; Zero-crossing Distortion; Value of Inductor; Phase Displacement; Parallel Interleaving

I. INTRODUCTION

In modern power electronics technology, Power Factor Correction (PFC) technology has been studied and applied widely. The input current is tracked with the input voltage strictly by the control circuits in PFC converters, so as to improve the power factor and suppress harmonic currents effectively. However, with the increase of the input frequency, the phenomenon of input current zero-crossing distortion would occurs, and the higher the input frequency is, the distortion phenomenon will be more serious [1].The airborne AC power system is 115V/400Hz, the distortion phenomenon is more obvious in this high-frequency and the THD is higher. It is faced with much difficulty to meet the harmonic current standard GJB181B-2012[2] in airborne system.

Single-phase PFC converter input current is ahead of the input voltage [3], and when the input frequency increases, the phase difference is increased accordingly, so near the input voltage zero crossing, input voltage and input current presence reverse. When the current is going to change, the result of one-way bridge rectifier diode conductivity is clamped to 0, waits until the input voltage starts to change direction, thus generating a current instantaneous step, generating zero-crossing distortion phenomenon.

Now researchers have proposed some solutions such as phase delay, the duty feedforward and so on. In some papers, by modeling the Boost PFC converter, the author added one voltage feed-forward network (LPAC) in the current control loop to reduce current phase advance. However, the whole design is more complex, and the phase difference is not the only reason so the control effect isn't obvious. The new structure of bridgeless topology is complex and difficult to control. What's more, the EMI problems are difficult to be solved effectively. This article focuses on the reasons of the zero-crossing distortion in Boost PFC converter, proposes a new method which is parallel interleaving technique to improve the zero crossing distortion, and uses simulation

software to demonstrate the theoretical analysis. Finally, the feasibility of this method is demonstrated by experiments.

II. THE REASONS OF THE ZERO-CROSSING DISTROTION

Assuming Boost PFC converter input voltage is $V_{in} = V_m \sin(2\pi ft)$, where V_m is the input voltage amplitude, f is the frequency of the input power. Ideally, Boost PFC converter input current is sinusoidal and in phase with the input voltage. By modeling the Boost PFC converter, it indicates that the input current phase is ahead of the input voltage and the higher the input higher the frequency is, the greater the retardation is[4]. Assuming the phase difference isθ, ideally $i_{idl} = \mathrm{I_m} \sin(2\pi ft + \theta)$. Input current distortion process is shown in Figure 1：

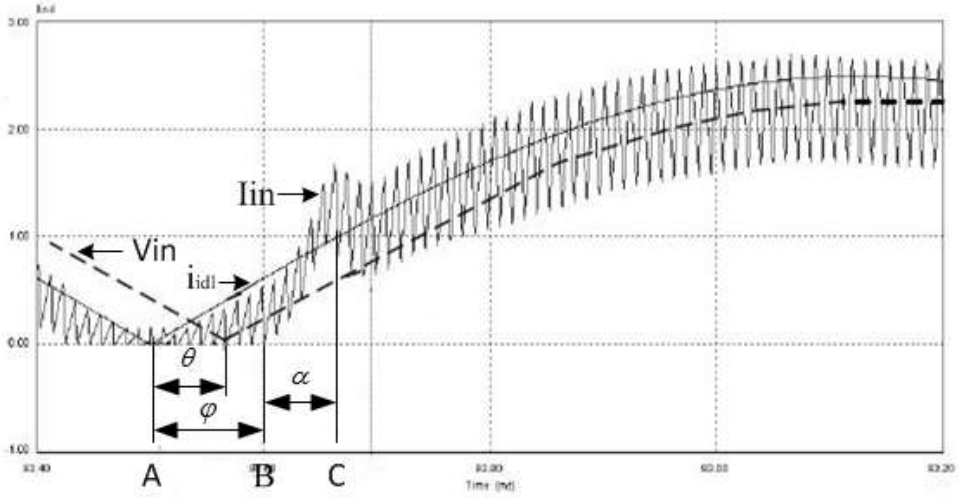


Figure-1: The input current distortion process

2.1 The converter operating in DCM mode

In the horizontal axis of AB interval, the converter operates in discontinuous mode. When the current is interrupted, the power gain level is lower than the one of continuous current, causing the gain of the current loop reducing, so that the input current is slow to respond, the inductor current is difficult to track the reference current. Supposing the DCM mode continues angle is φ,in the discontinuous mode boundary:

$$\begin{cases} \Delta I = \dfrac{(V_0 - V_{in})(1-D)}{L \cdot f_S} \\ \Delta \mathrm{I} = 2\mathrm{I}_0 / (1-D) \end{cases} \tag{1}$$

Simultaneous equation and replace π-φ to 2πft ,simplification is：

$$(V_0 - V_m \sin\varphi) \cdot V_m \sin\varphi = 2V_0 L f_S \cdot \mathrm{I_m} \sin(\varphi - \theta) \tag{2}$$

Order one function:

$$y_1(\alpha, f_S, \theta, L) = (V_0 - V_m \sin\varphi) \cdot V_m \sin\varphi - 2V_0 L f_S \cdot \mathrm{I_m} \sin(\varphi - \theta) \tag{3}$$

The function corresponding to the abscissa point is φ,Figure 2 depicts a graph of relationship graph when $\theta = 0°$ 、 $\theta = 5°$ ； f_S=100kHz 、 f_S=200kHz (when the specific parameters is $V_m = 163V, V_o = 390V, \mathrm{I_m} = 10A$).As can be seen from the figure, along with the increase, φ is also growing, and within range, the converter operates in DCM mode. After the increase of the switching frequency, φ is

significantly reduced. In order to reduce the converter operates in discontinuous mode of time, θ should be reduced and increase the switching frequency.

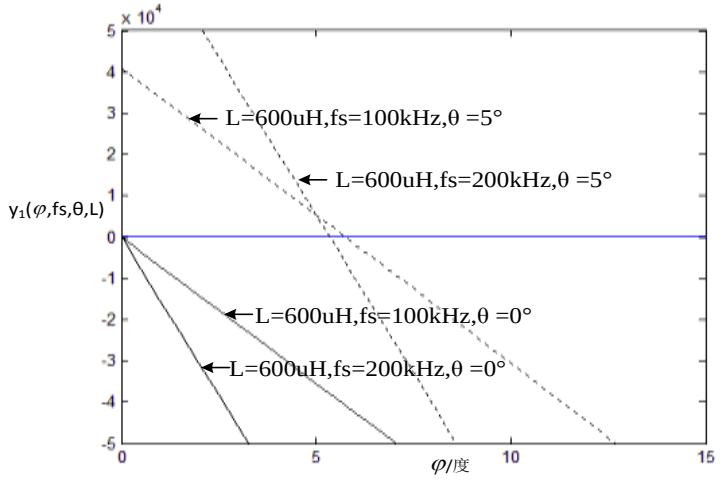


Figure-2: The Relationship Between φ and θ、fs

2.2 Cusp distortion

Seen in Figure 1, when the intermittent mode is ended, the inductor current sharp rise, there is a clear transition from B jump into C, at this stage the actual input current curve deviates from the ideal current track. Supposing the angle of cusp distortion is α , at this time on the ideal input current to derivate to obtain the desired increase in slope：

$$\frac{di_{idl}}{dt} = 2\pi f \cdot \mathrm{I_m} \cos(2\pi ft + \theta) \tag{4}$$

Obviously, the higher the power input frequency is, the rising slope converter needed is greater, so cusp distortion with increasing input frequency becomes more and more serious. According to Boost PFC circuit $di_L/dt = V / L$, at this time Boost PFC converter can provide for the inductor current rise rate is:

$$\frac{di_L}{dt} = V_m \sin(2\pi ft)/L \tag{5}$$

From Equation (5) it can be seen, the current rise rate that the converter provides is regardless of the input frequency, only a sense of the value of inductor. The smaller the inductance is ， the rising slope the converter provides is greater so it will be better able to track the input current over current curves. Integrate Equation (5), and order $i_L = i_{idl}$, the needed angle α that the inductor current tracking over ideal current is：

$$V_m(1-\cos\alpha)/2\pi fL = \mathrm{I_m}\sin(\alpha+\theta) \tag{6}$$

According to equation (6), order one function:

$$y_2(\alpha, f, \theta, L) = \frac{V_m(1-\cos\alpha)}{2\pi fL} - \mathrm{I_m}\sin(\alpha+\theta) \tag{7}$$

Function $y_2(\alpha, f, \theta, L) = 0$ corresponding to the abscissa point is that the function of the image as shown in Figure 3.As can be seen from the figure, when the input frequency is 50Hz, with an increase from 0 ° to 5 ° of θ, the α values are 1.5 ° and 3 °. When the input frequency increases to 400Hz, under the same circumstances, α becomes 10.5 ° and 14 °. α will increases as θ and f increase. But when the value of inductor reduces from 600uH to 280uH, α is down from 5 ° to 0.5 °. Thus at high input frequencies, in order to improve the current waveform, it is necessary to reduce α , so the value of inductor can be reduced to improve di/dt 。

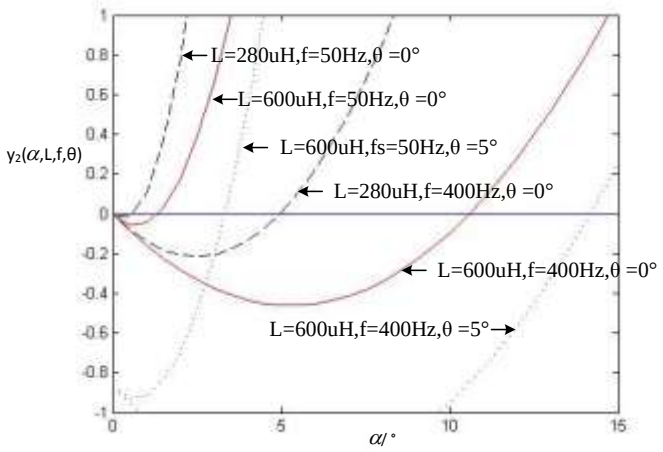


Figure-3:The Relationship Between α and L、θ、f

III. The INTRODUCTION OF PARALLEL INTERLEAVING TECHNOLOGY

From the above analysis, to reduce the zero-crossing distortion, it is need to reduce L and reduce θ. The value of the inductor is subject to the ripple current so it can't be reduced too much, otherwise the circuit will operate in DCM mode, exacerbate zero-crossing distortion. It is needed to improve the system current loop cut-off frequency to reduce θ, that requires a corresponding increase in switching frequency. The switching frequency is limited by the core material, the impact of driver chips and power devices, so it can't be increased indefinitely. Both the three-level technology and parallel interleaving technology can equivalently improve switching frequency and reduce the value of inductor without increasing the switching frequency of the system[6].Three-level technology is more complex and requires high stability of the system, so the parallel interleaving technology is used as PFC topology.

Figure 4 is the interleaved Boost PFC converter topology[7], it consists of two identical parameters Boost PFC converter units connected in parallel, two-way switch is in accordance with the duty cycle of the driving signal frequency, interleaving conduction 180°. The input current is the sum of the two inductor current and the output current is the sum of two boost diode current.

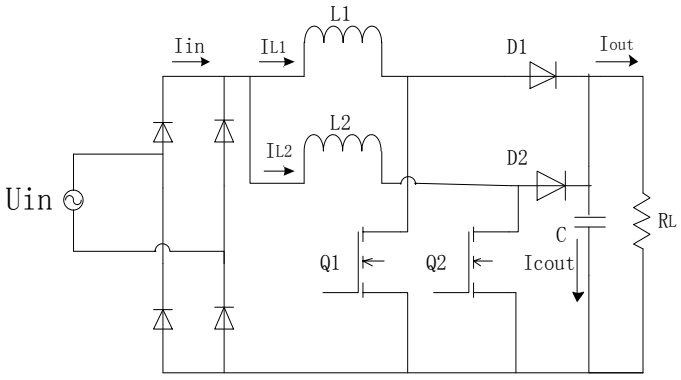


Figure-4:The block diagram of Interleaved Boost PFC

One obvious advantage of this topology is that two-way is interleaved, thus the equivalent switching frequency is doubled. Another advantage is that each branch of the inductor ripple current value of the coefficient can be larger, and thus reduce the value of inductor. Because the two inductors are in the conduction state of interleaving, so two phase inductor ripple current also in staggered state, two superimposed ripple

current can be cancelled to reduce input current ripple. Each branch provides current rising rate unchanged, but after two superimposed itself required input current rising slope was significantly reduced. Therefore the topology of the input current is easier to track the ideal current waveform, improving the input current zero-crossing distortion effectively.

IV. SIMULATION AND EXPERIMENTAL RESEARCH

Use simulation software TINA to simulate on the interleaved Boost PFC chip UCC28070 from TI . The experimental parameters are as follows：

(1) Input AC voltage: $V_{in}=115V/400Hz$;

(2) Output DC voltage: $V_o=390V$;

(3) Output power: $P_o=600W$;

(4) Inductance: $L_1=L_2=280uH$;

(5) Switching frequency: $f_S=200kHz$;

(6) Output capacitor: $C_0=360uF$.

As can be seen from the simulation Figure 5, the input current can track the input voltage very well, the phase difference is almost zero, the cusp distortion also improved much. The introduction of parallel interleaving technique can effectively improve the zero crossing distortion problems.

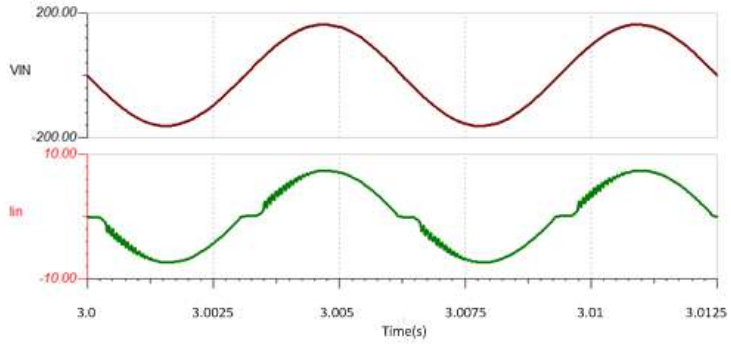
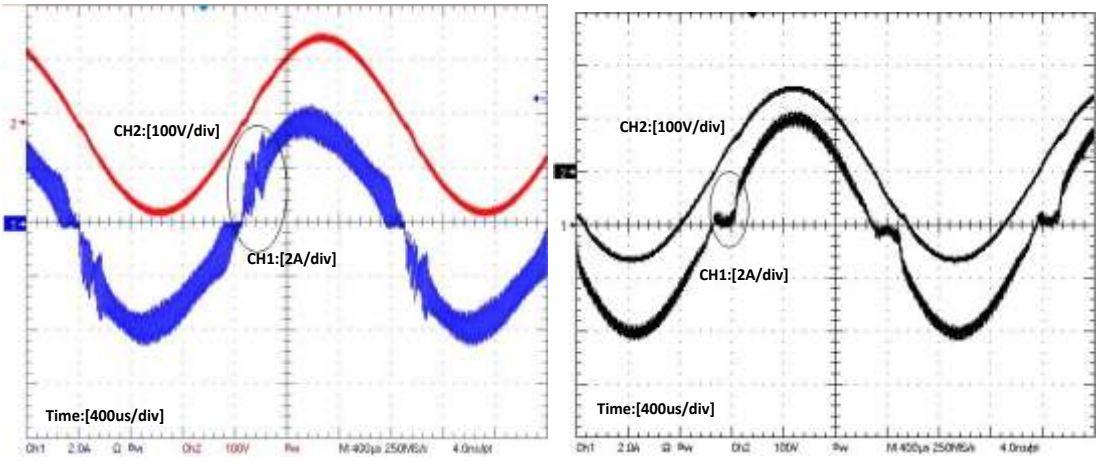


Figure-5:UCC28070 input voltage and input current simulation waveform

The laboratory already has a 600W Boost PFC experimental prototype which the controlling chip is IR1150, the peripheral circuit parameter： nductance $L=600uH$,switching frequency $f_S=100kHz$,output capacitor $C_0=360uF$.

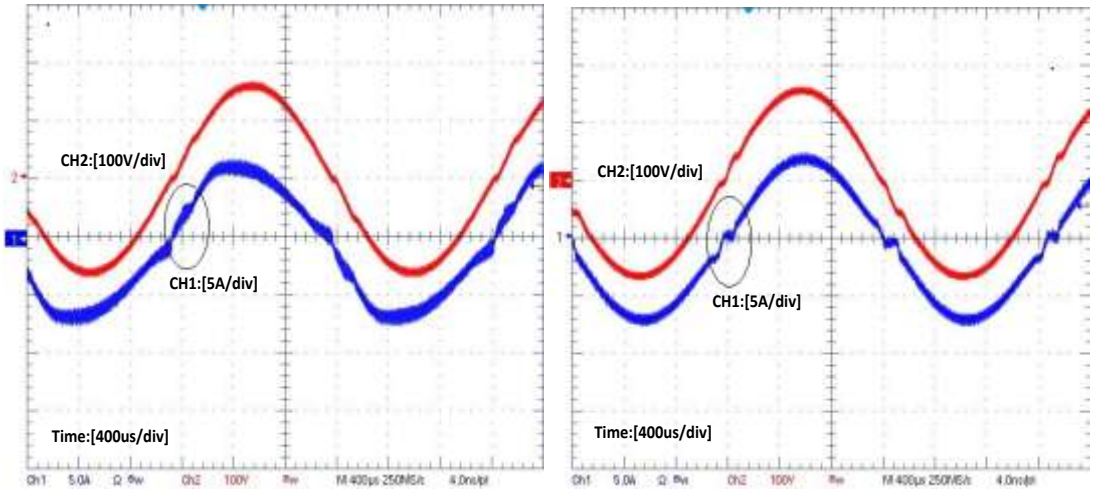
In order to verify the above analysis, the completion of a 600W interleaved Boost PFC prototype comparison, the controlling chip is UCC28070, experimental prototype parameters consistent with the simulation parameters. AC power supply box is Chroma 61504, power analyzer is Chroma 66202.

Experimental waveforms are as follows：



IR1150 UCC28070

Figure-6:The input voltage and current waveform under half load of two converters



IR1150 UCC28070

Figure-7: The input voltage and current waveform under full load of two converters

Figures 6, 7 are given half load、full load Boost PFC converter input voltage and the input current waveform. It can be seen from the waveform, using IR1150 of Boost PFC converter input voltage crosses zero phase advance angle is large, and α is also larger, it has more serious current distortion so the current ripple is larger. And after using interleaved Boost PFC converters, there is almost no phase difference and α is significantly reduced, compared to the Boost PFC converter current harmonics is also greatly reduced, THD and PF values are shown in Table 1, each input current harmonics can meet the appropriate standards.

Table 1 The PF and THD of the two converters at half and full load

	PF/THD	IR1150	UCC28070
300W	PF	0.9831	0.9962
	THD	7.9390%	4.8619%
600W	PF	0.9865	0.9949
	THD	8.7137%	4.9764%

V. CONCLUSION

By analyzing Boost PFC converter input current zero distortion causes, the derived solution is to reduce the value of inductor and improve higher switching frequencies. Interleaved technology because of its topological characteristics can reduce value of inductor and the equivalent switching frequency is doubled. From both simulation and experimental prototype to verify that the use of this Boost PFC converter topology can effectively improve the input current zero-crossing distortion to meet the corresponding current harmonic standards.

VI. Acknowledgements

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